

MOS FIELD EFFECT TRANSISTOR NP88N055CLE, NP88N055DLE, NP88N055ELE

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance

RDS(on)1 = 5.2 m Ω MAX. (VGS = 10 V, ID = 44 A)

RDS(on)2 = $6.3 \text{ m}\Omega$ MAX. (VGS = 5.0 V, ID = 44 A)

- Low Ciss : Ciss = 9700 pF TYP.
- Built-in gate protection diode

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage	Voss	55	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC) Note1	ID(DC)	±88	Α
Drain Current (Pulse) Note2	D(pulse)	±352	Α
Total Power Dissipation (T _A = 25°C)	Рт	1.8	W
Total Power Dissipation (Tc = 25°C)	Рт	288	W
Single Avalanche Current Note3	las	75 / 88	Α
Single Avalanche Energy Note3	Eas	562 / 232	mJ
Channel Temperature	Tch	175	°C
Storage Temperature	T_{stg}	-55 to +175	°C

- Notes 1. Calculated constant current according to MAX. allowable channel temperature.
 - **2.** PW \leq 10 μ s, Duty cycle \leq 1 %
 - 3. Starting T_{ch} = 25°C, R_G = 25 Ω , V_{GS} = 20 V \rightarrow 0 V (See Figure 4.)

THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	0.52	°C/W	
Channel to Ambient	Rth(ch-A)	83.3	°C/W	

ORDERING INFORMATION

PART NUMBER	PACKAGE
NP88N055CLE	TO-220AB
NP88N055DLE	TO-262
NP88N055ELE	TO-263

(TO-220AB)



(TO-262)



(TO-263)



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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

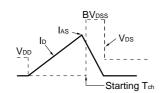


ELECTRICAL CHARACTERISTICS (TA = 25°C)

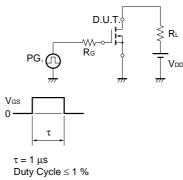
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CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)1	Vgs = 10 V, ID = 44 A		4.1	5.2	mΩ
	RDS(on)2	Vgs = 5.0 V, ID = 44 A		4.8	6.3	mΩ
	RDS(on)3	Vgs = 4.5 V, ID = 44 A		5.1	6.8	mΩ
Gate to Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \mu\text{A}$	1.5	2.0	2.5	٧
Forward Transfer Admittance	yfs	V _{DS} = 10 V, I _D = 44 A	38	75		S
Drain Leakage Current	Ipss	Vps = 55 V, Vgs = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	V _G S = ±20 V, V _D S = 0 V			±10	μΑ
Input Capacitance	Ciss	V _{DS} = 25 V		9700	14600	pF
Output Capacitance	Coss	Vgs = 0 V		1100	1700	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		490	890	pF
Turn-on Delay Time	td(on)	ID = 44 A		37	82	ns
Rise Time	t r	V _{GS(on)} = 10 V		22	56	ns
Turn-off Delay Time	td(off)	V _{DD} = 28 V		180	360	ns
Fall Time	t f	$R_G = 1 \Omega$		35	88	ns
Total Gate Charge 1	Q _{G1}	ID = 88 A, VDD = 44 V, VGS = 10 V		160	240	nC
Total Gate Charge 2	Q _{G2}	ID = 88 A		88	140	nC
Gate to Source Charge	Qgs	V _{DD} = 44 V		27		nC
Gate to Drain Charge	Q _{GD}	Vgs = 5.0 V		48		nC
Body Diode Forward Voltage	V _{F(S-D)}	IF = 88 A, VGS = 0 V		1.0		٧
Reverse Recovery Time	trr	IF = 88 A, VGS = 0 V		62		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		120		nC

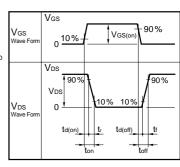
TEST CIRCUIT 1 AVALANCHE CAPABILITY

$\begin{array}{c|c} D.U.T. \\ \hline \\ PG. \\ \hline \\ V_{CS} = 20 \rightarrow 0 \\ \hline \end{array} \begin{array}{c} D.U.T. \\ \hline \\ \hline \\ \hline \\ V_{DD} \\ \hline \end{array}$



TEST CIRCUIT 2 SWITCHING TIME





TEST CIRCUIT 3 GATE CHARGE

TYPICAL CHARACTERISTICS (TA = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

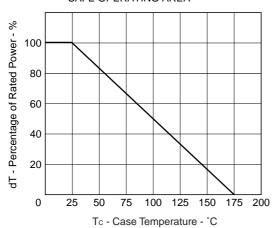


Figure.3 FORWARD BIAS SAFE OPERATING AREA

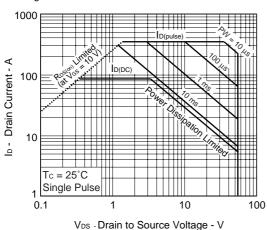


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

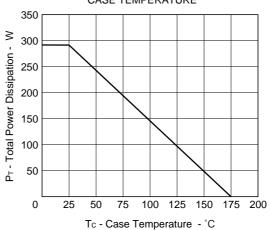
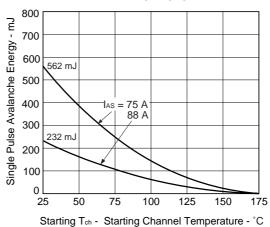


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR



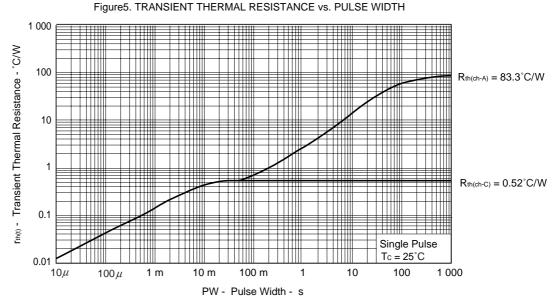


Figure 6. FORWARD TRANSFER CHARACTERISTICS

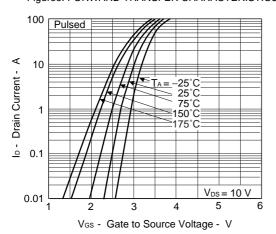


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

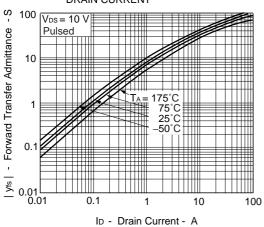


Figure 10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT $\mathsf{Rbs}_{\text{(on)}}$ - Drain to Source On-state Resistance - $\mathsf{m}\Omega$ 15 10 5.0 V Vgs = 4.5 V 10 V 5 0 100 1000

ID - Drain Current - A

Figure 7. DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

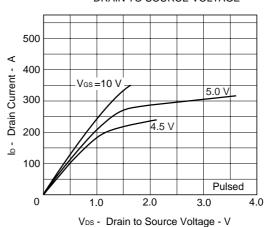


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

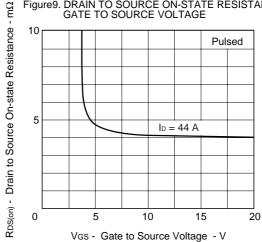
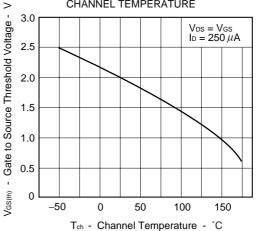


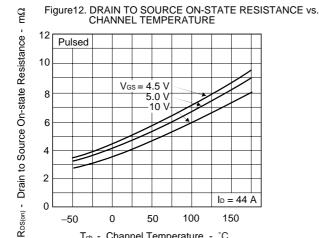
Figure 11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



0

-50

0



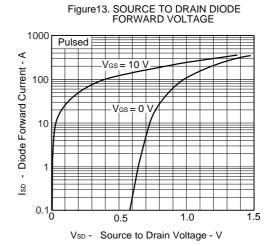
50

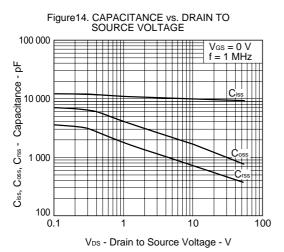
 $T_{\text{ch}}\,$ - $\,$ Channel Temperature - $\,^{\circ}\text{C}\,$

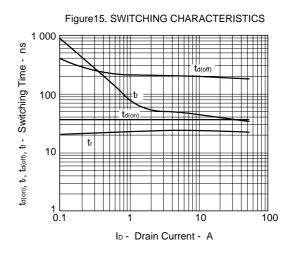
100

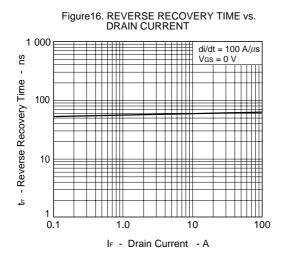
 $I_D = 44 A$

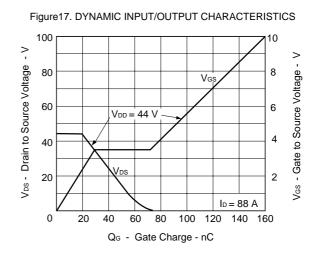
150





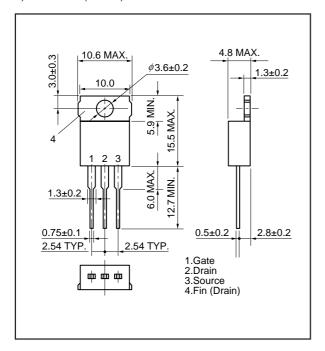




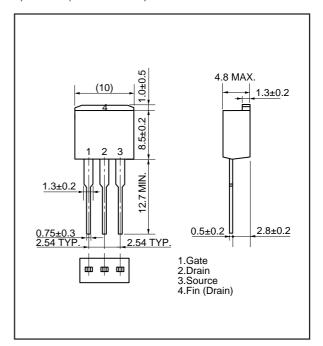


PACKAGE DRAWINGS (Unit: mm)

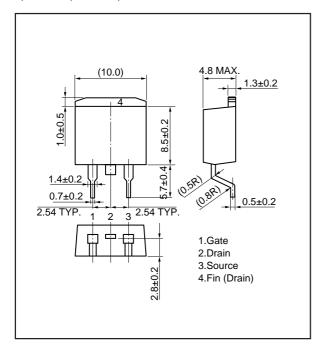
1) TO-220AB (MP-25)



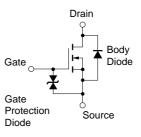
2) TO-262 (MP-25 Fin Cut)



3) TO-263 (MP-25ZJ)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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